Agilent E4430B 1 GHz, E4431B 2 GHz, E4432B 3 GHz, E4433B 4 GHz

Measuring Bit Error Rate Using the ESG-D Series RF Signal Generators, Option UN7

Product Note

Introduction

Bit-error-rate analysis

As digital communication technologies continue to evolve, the measurement of bit error rate (BER) increases in importance. BER is used in a variety of applications, such as sensitivity and selectivity measurements for receivers, components, or subsystem characterization.

To keep pace with the demanding requirements of the rapidly changing communications market, manufacturers and designers need equipment that is compact, easy to use, and provides basic capabilities for common measurements, such as BER.

Leading the way, Agilent ESG-D series RF signal generators provide an optional internal BER analyzer (Option UN7). This feature offers generic BER analysis capabilities for demodulated PN9 and PN15 data sequences that meet ITU-T standards.

This product note introduces BER measurement using the ESG-D series, and discusses the following topics:

- Bit-error-rate testing basics
- ESG-D series BER functions
- Measurement configurations
- ESG-D series BER operation

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Bit-error-rate testing basics

Basic BERT model

Bit error rate is measured by comparing the bit sequence output from a receiver with a known reference bit sequence.

In the basic BERT model shown in figure 1, a bit pattern is encoded on the signal and then transmitted to the receiver through the transmission channel. The receiver feeds the demodulated bit stream to a comparator where it is compared with the reference bit sequence. Delay is added to the path of the reference bit sequence as needed to synchronize the reference bit stream with the receiver's decoded bit stream.

Synchronizing the bit streams is usually the most challenging aspect of this test method. This challenge can be eliminated by using a pseudorandom bit sequence as the test signal. This method is discussed in the following section.

BERT using Pseudorandom Bit Sequence (PRBS)

The two most common pseudorandom bit sequences used for BER analysis of communication systems are PN9 and PN15. PRBS signals are defined by their length: PN9 is a 511-bit (2^9-1) sequence, and similarly, PN15 is a 32,767-bit ($2^{15}-1$) sequence. PRBSs are unique because a 9- or 15-bit sequence never repeats during the entire corresponding 511 or 32,767-bit sequence. As a result, the PRBS test signal has the transmission characteristics of a randomly created signal. However, unlike randomly created signals, all subsequent bit sequences can be determined from any 9-bit sequence for PN9 or 15-bit sequence for PN15.

This unique property makes it possible to reconstruct the subsequent portion of the 511- or 32,767-bit stream from the initial and correctly received 9 or 15 bits. Subsequently received bits are then compared with the reconstructed bit stream. This eliminates the need to directly compare the received and transmitted bits, consequently eliminating the need for synchronization of the received and reference bit streams.

The BERT must receive and correctly demodulate at least one 9- or 15-bit sequence in order to reconstruct the entire 511- or 32,767-bit sequence. Therefore, a system with an error rate over 11 percent (1/9) cannot start a measurement because bit-stream reconstruction is impossible. Similarly, the upper limit of the PN15 is 6.7 percent (1/15) error rate.

Figure 2 shows the measurement system with PRBS.

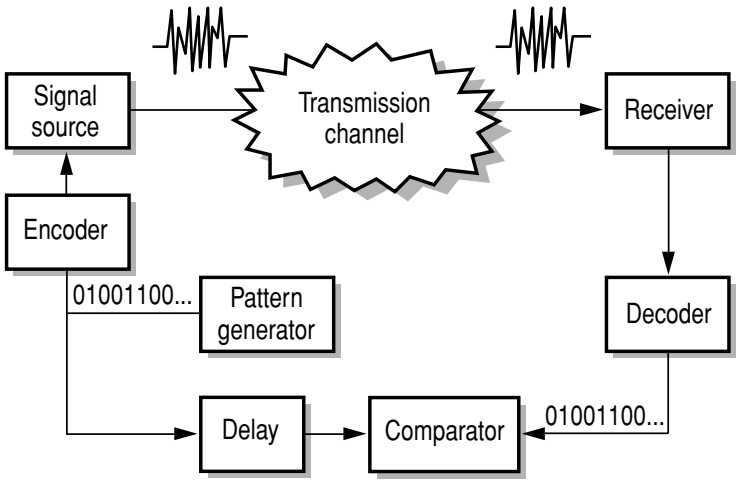

Figure 1. Basic BERT model

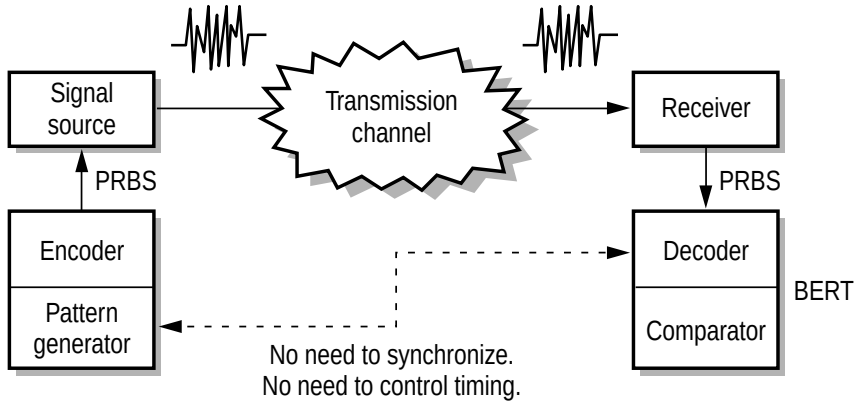

Figure 2. BERT using a PRBS

Comparing baseband BER and loopback BER

There are two methods of measuring the BER of mobile phones: baseband BER and loopback BER. The UUT feature set dictates which BERT measurement to use.

With the baseband method, the demodulated signal at the receiver remains at baseband frequencies and is routed to the comparator for comparison with the reference signal. Typically PDC and PHS phones and subassemblies use the baseband BER measurement method.

As the term loopback suggests, the received signal is "looped back" or retransmitted back to the receiver associated with the original transmitter for evaluation. Within the UUT, the signal is completely demodulated to the baseband bit-stream before being re-encoded and retransmitted. Comparison between the bit stream routed through the receiver and the reference signal takes place within the test device—usually a base station. GSM UUTs use the loopback BER measurement method.

Agilent ESG-D series configuration

The ESG-D series signal generator must be equipped with an internal I/Q baseband generator (Option UN8, UN3, or UN4) to support the internal BER analysis option. For transmission, the internal I/Q baseband generator creates the RF signal to be sent to the UUT. In some cases, the optional dual arbitrary waveform generator (Option UND) can be used to create the RF signal to be sent to the UUT; however, an internal baseband I/Q generator is still required to support the internal BER analysis option. Option UN7 is used to receive and analyze the baseband signal from the UUT.

Option UN7 can be used as a stand alone BERT for externally generated PN9 and PN15 sequences that meet ITU-T standards; however, an internal baseband I/Q generator is still required to support the internal BER analysis option.

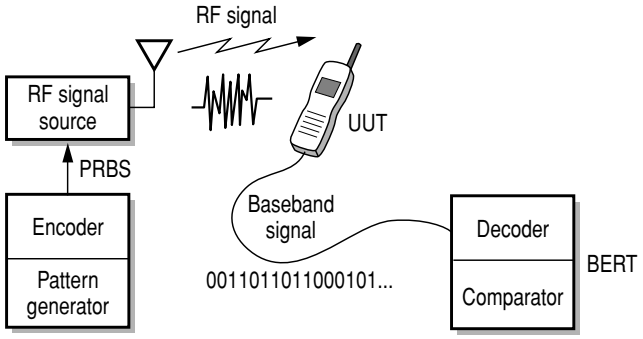

Figure 3. Baseband BERT

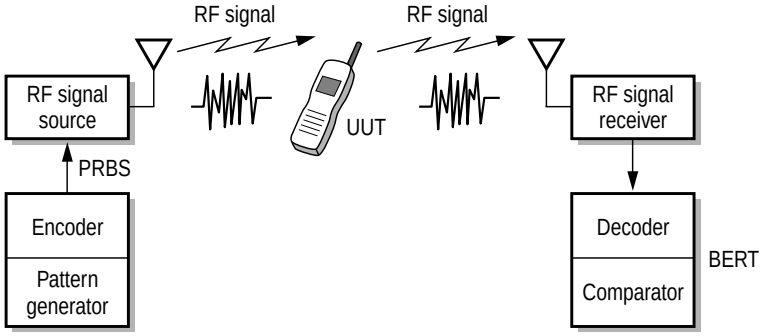

Figure 4. Loopback BERT

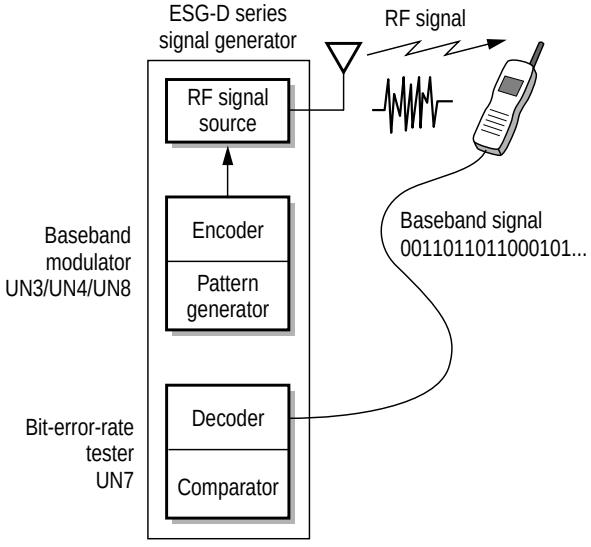

Figure 5. Agilent ESG-D BERT configuration

Agilent ESG-D series BER functions

Maximum data-rate selection of 2 Mbps or 10 Mbps

The ESG-D series Option UN7 has two maximum-data-rate modes: 2 Mbps and 10 Mbps. Data rates from 100 bps to 10 Mbps are acceptable. Each mode also has the following strengths:

2 Mbps mode

- Real-time display of
  - – total bits counted
  - – total bit errors detected
  - – current BER
- Suitable for testing most mobile phones
- Pass/Fail indication
- Automatic resynchronization
- Special pattern ignore function

10 Mbps mode

- Real-time display of total bits counted
- Suitable for testing higher data rate
- Pass/Fail indication

Pass/Fail indicator

The signal generator's Pass/Fail indicator is large and easy for inspectors to read.

You can select the Pass/Fail display update mode to be at cycle end or fail hold. Cycle end mode updates the indicator every measurement cycle. This method permits real-time UUT evaluations or adjustments. Fail hold mode maintains fail result until the next trigger. This mode is useful to determine when the failure occurred.

No Data/No Clock display

The BER analyzer automatically indicates "No Clock" when the clock input signal does not change for three seconds. "No Data" will be indicated when the data input signal does not change for 200 clocks. This function avoids erroneous measurements caused by improper connections or incorrect UUT settings.

Real-time display update (2 Mbps mode only)

The ESG-D series displays total bits counted, total bit errors detected, and the current bit error rate while measuring BER. Observe the results real-time or upon completion.

Automatic resynchronization

Turning on this function automatically resynchronizes the PRBS sequence when BER exceeds a threshold level. It is useful for continuously testing without triggering at every reconnection of the UUT.

Turning off this function continues the BER measurement without re-synchronization as long as the clock signal continues. This means that the ESG-D series can measure high BER once clock/data synchronization is established.

Selectable input impedance (TTL or 75 ohm)

Clock/Data input impedance is selectable at either TTL compatible or 75 ohm to match other test equipment.

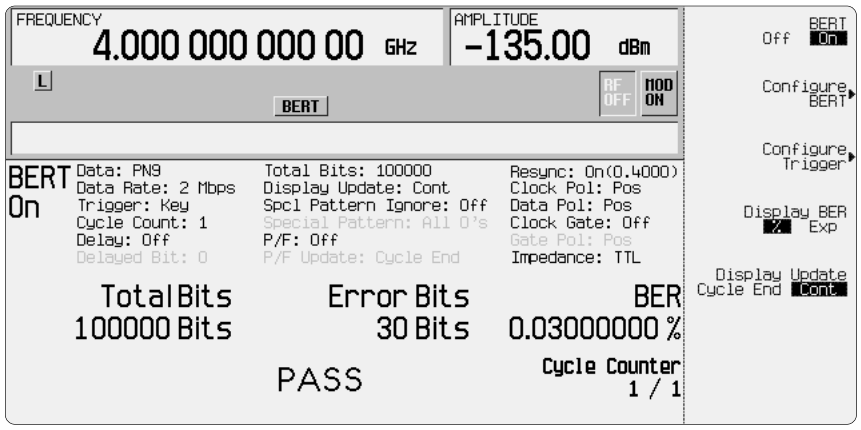

Figure 6. Agilent ESG-D series RF signal generator BERT user interface

Special pattern ignore
Some types of UUTs generate continuous 0 or 1 output data when they receive an unreadable RF signal. Measuring BER of such a data pattern gives a different result from the UUT's real performance. Ignoring this pattern gives an accurate measurement of the UUT. The ESG-D series BERT has a capability to ignore sequential 0s or 1s over 160 bits long.

This capability is called the "Unique Word Error Correction" function in PHS testing. When a PHS mobile cannot receive the unique word (UW) during signal reception, the mobile drops all the TCH data of the frame in which the UW error occurs. The special pattern ignore function complies with PHS operation.

Clock gate input
There are two ways to control the data stream with the ESG-D series BER analyzer. The implementation is dependent on the UUT. If the clock is on only when the data is valid, as depicted in figure 7, the bits will only be input for analysis when the clock is on.

Alternatively, the ESG-D series BER analyzer has a clock-gate input terminal that can be used to strip away a framed signal for recognition by the BER analyzer.

This is useful for UUTs in which the clock is constantly on. The gate is used to gate the clock from the UUT into the BERT. The BER analyzer accepts the clock signal when the gate is active, as shown in figure 8. Figure 9 shows an example of a PHS frame structure and the required clock-gate signal to extract TCH from the PHS framed pattern.

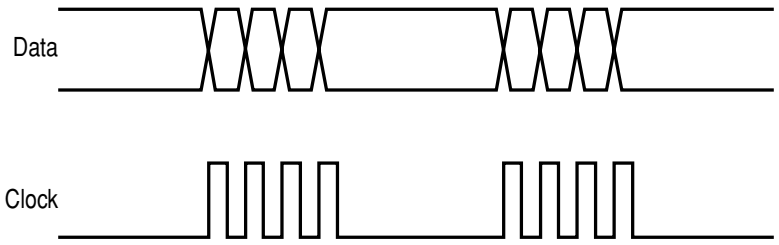

Figure 7. Bursted data and clock

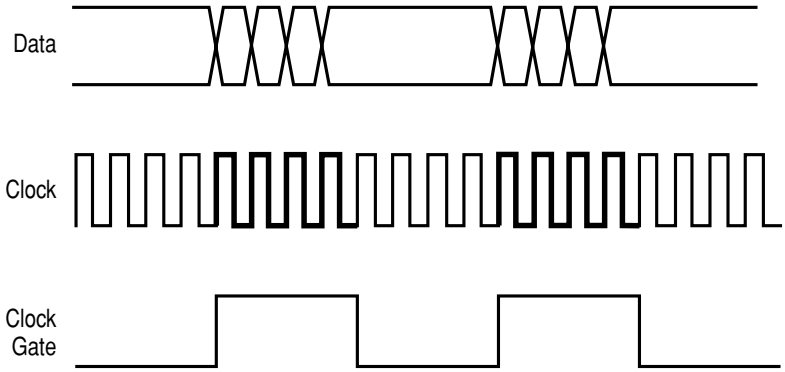

Figure 8. Gated clock and data

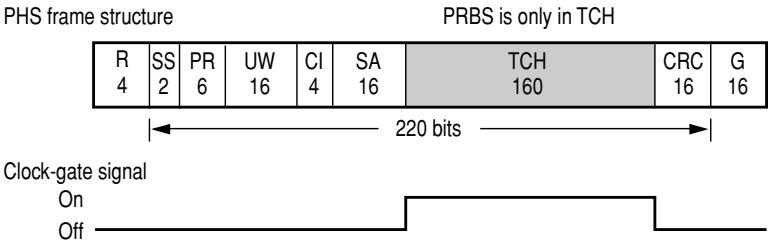

Figure 9. PHS frame structure and clock-gate signal

Measurement configurations

Typical configuration

Prepare an interface box that connects a controller and the UUT, and convert Data/Clock impedance and level to TTL. Connect the controller to the control terminal of the UUT interface box as shown in figure 10.

Connect data and clock signal from the UUT interface box to BER DATA IN and BER CLK IN terminals on the rear panel of the ESG-D series, respectively. Set the ESG-D series input impedance to match the interface box output impedance with the following key operation.[1] [BERT] ▶Configure BERT]▶ [More (1 of 3)]▶[More (2 of 3)]▶ [Impedance]

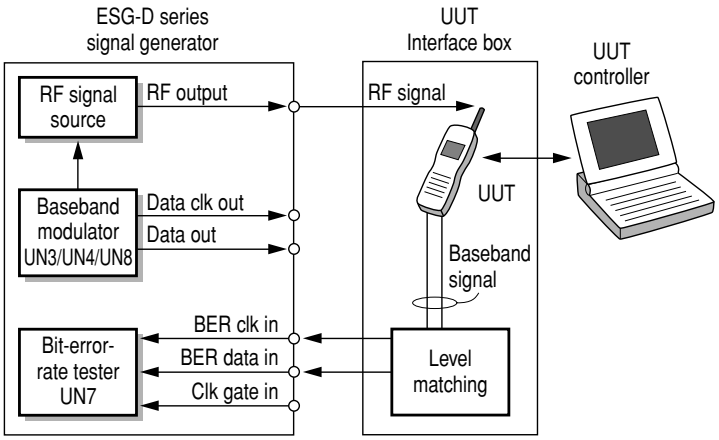

Figure 10. Typical test configuration

Gated signal configuration

The ESG-D series BER has a BER GATE IN input. This is used to gate the BER CLK IN signal. The clock signal is valid only when the clock-gate input is active. If the clock and data from the UUT need to be gated, connect the clock-gate signal from the interface box to BER GATE IN terminal. Then validate the BER GATE IN input by the following key operation. [BERT]▶ [Configure BERT]▶[More (1 of 3)]▶[More (2 of 3)]▶[Clock Gate]. Figure 11 is a configuration for this type of measurement.

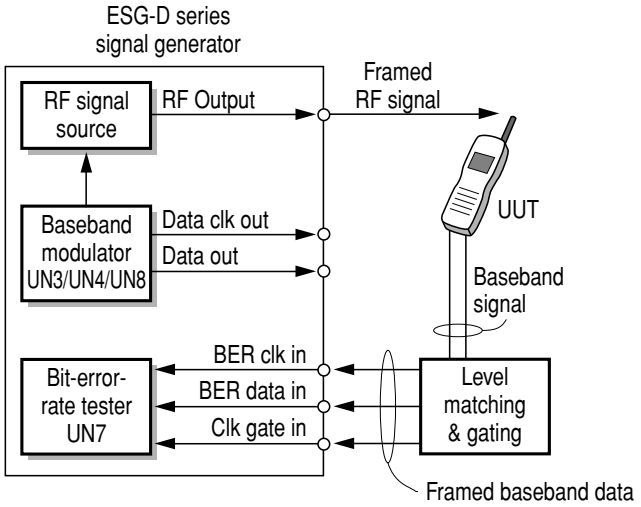

Figure 11. Gated test configuration

Unframed signal test with self-clocking

Figure 12 is an example for a UUT that simply receives an unframed RF signal and demodulates it to obtain a baseband signal. When measuring BER, a clock signal that corresponds to the UUT's output data must be input to the BER CLK IN. If the clock is not available from the UUT use the DATA CLK OUT signal from the ESG-D series baseband modulator (Options UN3, UN4 or UN8). If this clock is used, a delay must be added to correspond to the UUT's processing time.

1. Words within square brackets represent a softkey function.

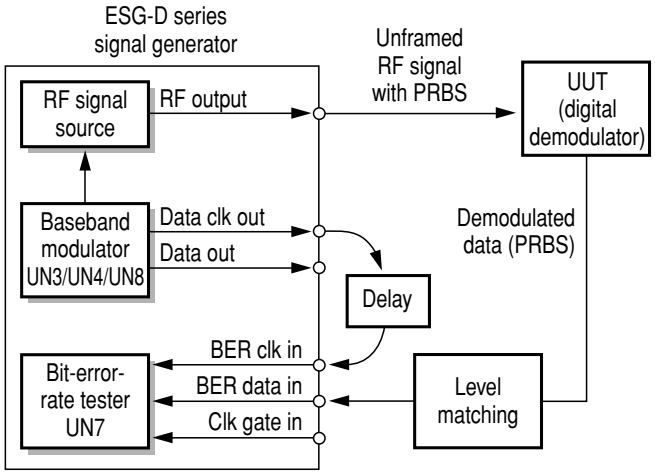

Figure 12. Unframed signal test configuration

Agilent ESG-D BER operation

1. Activate the UUT

Set the UUT to test mode as required. Depending on the UUT type, an external controller may be needed to interface with the ESG-D series.

2. Setup ESG-D series

After pushing the Mode hardkey, push the [BERT]▶softkey.

3. Configure BERT

Configuring BERT means setting up the data, thresholds, and connectivity.

Press [Configure BERT]▶. This accesses three softkey screens to complete the configuration. The screens are shown in figures 13 through 15.

4. Data: set the maximum data type, data rate, and total bit count

The softkey choices are shown in figure 13.

Press [Data]▶. Select PN9 or PN15.

Press [Max. Data Rate]▶. Select 2 Mbps or 10 Mbps. The default is 2 Mbps.

Press [Total Bit]. Specify how many bits will be measured in one measurement cycle using the keypad or knob. The default is 10,000 bits.

5. Thresholds: determine use of the Pass/Fail indicator

Press [More (1 of 3)] The softkey choices are shown in figure 14.

Press [Pass/Fail], choose Off or On.

If On is selected two additional set-ups are required. Set the Pass/Fail Limit and the Pass/Fail Update

Press [Pass/Fail Limit], specify the number of error bits required for a fail in using the keypad or knob. Select the dimension to be a percentage or parts per million The default is 0.01.

Press [Pass/Fail Update], select Cycle End or Fail Hold. The default is cycle end.

6. Connectivity: set clock parameters and impedance

Press [More (2 of 3)]. The softkey choices are shown in figure 15.

Press [Clock Polarity]. Choose Negative or Positive.

Press [Data Polarity]. Choose Negative or Positive.

Press [Clock Gate]. Choose Off or On.

Press [Impedance]. Choose 75 ohm or TTL.

Return to the BERT menu.

7. Configure initiation of measurement

Press [Configure Trigger].

Press [BERT Trigger]. Select immediate, Trigger key, Bus or External.

Return to the BERT menu.

8. Start the measurement

Press [BERT]▶[BERT Off On] to turn BERT Mode On.

Press [Trigger] key on the ESG-D series front panel to start BER measurement if trigger was the chosen BERT initiation.

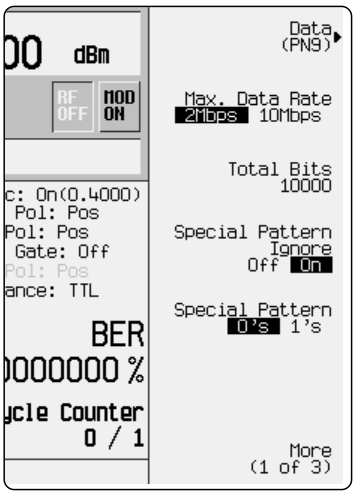

Figure 13. Configure BERT menu 1 of 3

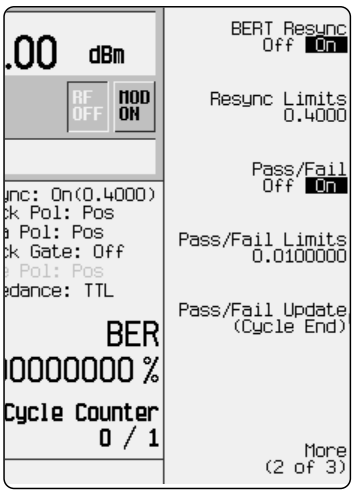

Figure 14. Configure BERT menu 2 of 3

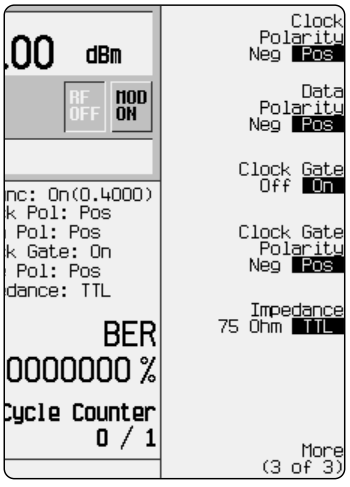

Figure 15. Configure BERT menu 3 of 3

9. Display measurement result
Total bits, error bits, and BER are displayed as shown in figure 16. If the following annunciators are displayed before starting the measurement, check that the UUT setting is proper.

- No Data: Data cable is not connected properly or data has not changed for more than 200 clock signals.
- No Clock: Clock cable is not connected properly or clock signal is not present for more than 3 seconds.
- Sync Loss: ESG-D BER tester cannot establish PRBS synchronization. BER is very high even though data and clock are both normal. Possible causes are wrong data type selection between PN9 and PN15, or wrong polarity selection of data and clock signals.

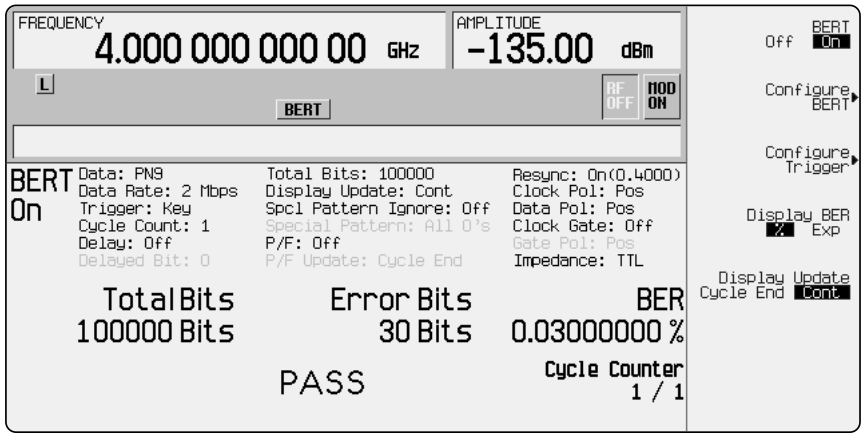

Figure 16. BER analyzer display

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